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APPLICATION NUMBER: *60/456,770*
FILING DATE: *March 21, 2003*
RELATED PCT APPLICATION NUMBER: *PCT/US04/08724*

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03/21/03 JC670 U.S. PTO

U.S. PTO 60/456770

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EV281802230US

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Mark Alan LaMonte	Johnson	Raleigh, NC
Douglas William	Barlage	Raleigh, NC
John	Muth	Raleigh, NC

☐ *Additional inventors are being named on the _____ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

LATERAL OVERGROWTH OF NANOSCALE LITHOGRAPHICALLY PATTERNED SEMICONDUCTOR DEVICES FOR ELECTRONIC, PHOTONIC, MOLECULAR-ELECTRONIC AND SPINTRONIC APPLICATIONS

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ENCLOSED APPLICATION PARTS (check all that apply)

☒ Specification *Number of Pages* 13

☐ Drawing(s) *Number of Sheets*

☐ Application Data Sheet. See 37 CFR 1.76

☐ CD(s), Number

☐ Other (specify)

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☒ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees

☐ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number:

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE AMOUNT ($): 80.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE _____ Date 3-21-03

TYPED or PRINTED NAME Gregory A. Hunt

TELEPHONE 919-493-8000

REGISTRATION NO. (*if appropriate*) 41,085

Docket Number: 297/172

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S.D Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

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March 21, 2003

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Date of Deposit: March 21, 2003
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Shayler E. Dunn

Commissioner for Patents
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Washington, D.C. 20231

Re: U.S. Provisional Patent Application for LATERAL OVERGROWTH OF NANOSCALE LITHOGRAPHICALLY PATTERNED SEMICONDUCTOR DEVICES FOR ELECTRONIC, PHOTONIC, MOLECULAR-ELECTRONIC AND SPINTRONIC APPLICATIONS
Our File No. 297/172

Sir:

Please find enclosed the following:

1. A U.S. provisional patent application for LATERAL OVERGROWTH OF NANOSCALE LITHOGRAPHICALLY PATTERNED SEMICONDUCTOR DEVICES FOR ELECTRONIC, PHOTONIC, MOLECULAR-ELECTRONIC AND SPINTRONIC APPLICATIONS (13 pages);

2. Provisional Application for Patent Cover Sheet (Form PTO/SB/16) in duplicate;

3. A return-receipt postcard to be returned to our offices with the U.S. Patent and Trademark Office date stamp thereon; and

4. A Certificate of Express Mail No.: EV281802230US.

Please contact our offices if there are any questions.

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account Number **50-0426**.

Respectfully submitted,

JENKINS & WILSON, P.A.

Gregory A. Hunt
Registration No. 41,085
Customer No. Bar Code Label:

25297
PATENT TRADEMARK OFFICE

GAH/sed

Enclosures

CONFIDENTIAL *(NCSU Patent Office Use Only)*
NCSU File No. _____
Lawyer's File No. _____

NCSU INVENTION DISCLOSURE FORM

This form must be signed by the Department Head and the College Dean/Associate Dean prior to submission:

Inventor's Name: Johnson, Mark Alan LaMonte — Citizenship: USA
Title: Asst. Professor — Department: MSE
Mailing Address: Box 7907, Raleigh, NC 27695-7907 — Telephone: 513-2480
Social Security No: 473-72-2655

Inventor's Name: Barlage, Douglas William — Citizenship: USA
Title: Asst. Professor — Department: ECE
Mailing Address: 234-F EGRC, Raleigh, NC 27695 — Telephone: 513-3018
Social Security No: 268-64-1880

Inventor's Name: Muth, John — Citizenship: USA
Title: Asst. Professor — Department: ECE
Mailing Address: 234-D EGRC, Raleigh, NC 27695 — Telephone:
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Inventor's Name: — Citizenship:
Title: — Department:
Mailing Address: — Telephone:
Social Security No:

Inventor's Name: — Citizenship:
Title: — Department:
Mailing Address: — Telephone:
Social Security No:

1. Title of Invention: Lateral Overgrowth of Nanoscale Lithographically Patterned Semiconductor Devices for Electronic, Photonic, Molecular-Electronic and Spintronic Applications

2. Date Invention Conceived (Conception Date): _____

3. Has the Invention been reduced to practice? ☐ Yes No

4. Supporting Data Notebook No. _____
   Pages _____

5. Has the Invention been published: Orally No In writing No
   a. When: _____
   b. Authors: _____
   c. Any changes in the Invention since public disclosure (please attach copies of any publications, if available): _____

6. Brief Description. Is the Invention a new process, composition of matter, a device or one or more products? A new use for, or an improvement on an existing process. Please describe.
   Invention is a process for the epitaxial growth of photolithographically patterned nanoscale feature arrays in semiconductors, metals, ferroelectrics or insulators. Application of this innovative technique enables a multitude of farication processes for the practical manufacturing of electronic, photonic, spintronic, molecular electronic or nano- mechanical systems. This innovative process enables fabrication processes to meet the spatial requirements projected in the ITRS roadmap. (Moore's Law.) Device descriptions included as well as process descriptions.
   [Detailed Description of Innovation is Attached]

   (Insert additional sheets to elaborate or attach descriptive material before page 4.)

7. Write a brief descriptive abstract of your Invention without making a disclosure. This will be used for marketing purposes.
   This invention describes novel epitaxial growth methods and structures to achieve nanoscale spatial dimensions for the active and passive layers of semiconductor devices, (particularly wide bandgap III-Nitride semiconductors), and the incorporation of these processes into interconnect and active layer device fabrication processes. Extension of these methods to the nanometer spatial domain is a critical enabling technology for the practical realization of electronic, photonic, molecular-electronic, spintronic and nano-mechanical (NEMS) devices which have been proposed for this spatial scale.

8. From the description, pick out and expand on novel and unusual features. How does the Invention differ from present technology? What problems does it solve or what advantages does it possess?
   1.) Use of lateral epitaxial growth of III-Nitride semiconductors to the problem of active device layer fabrication or device interconnection layer fabrication in semiconductor devices on the nanometer scale. (Lateral growth has previously been employed for heteroepitaxial matching and the growth of low-defect substrates for these materials.)
   2.) Use of edge definition lithography with multiple parallel features to achieve nanometer scale patterning with multiple parallel features prior to epitaxial regrowth. (Edge definition lithography or 'spacer gate' lithography has previously been used to define individual features in the nanometer spatial scale.) The ability to fabricate arrays of nanometer scale features using conventional optical lithography will enable the practical realization of many proposed structures and is the subject of a separately filed intellectual property disclosure at NCSU.

3.) Controlled lateral epitaxial overgrowth on the nanometer spatial scale. (Previous lateral growth has been performed with masking [or trench pseudo-masking] and regrowth on the micrometer spatial scale.) The primary emphasis in previous lateral overgrowth art has been as a process to achieve a reduction in crystal growth defects. (The specific defects are called 'dislocations' and arise due primarily as the result of misregistry strain during epitaxial growth.) In a process for defect density reduction, the nanometer spatial scale is less than the spacing between dislocation defects and hence provide a beneficial improvement in material quality. Techniques of random 'self-assembed' masking on the nanometer scale has shown to be of benefit in dislocation reduction as well as the controlled micrometer scale masking prior to epitaxial regrowth.

4.) For active device and interconnect layers, the nanometer spatial scale is consistent with projected device feature sizes of the ITRS (Silicon technology roadmap) and hence may be the key technology for extending Moore's law in the 8-12 year time horizon. For molecular electronics, this spatial scale is consistent with the requisite interconnect distances of the active molecules. For photonic crystals, periodic arrays on this feature size is consistent with the formation of photonic bandgap materials in the visible and ultraviolet wavelength range. For each of these, the availability of practical fabrication processes are currently key limiting factors and roadblocks in the achievement of technological advances.

9. In not indicated previously, what are possible uses for the Invention? In addition to immediate applications are there other uses that might be realized in the future?

1.) Fabrication and integration of semiconductor digital logic chips meeting Moore's Law requirements in the 8-12 year time horizon. (Full scale production in 2010-2014)
2.) Molecular electronic device interconnect technologies
3.) Visible, IR and UV photonic bandgap crystals (addressing current needs)
4.) Multiple nanoscale fabrication applications
5.) RF, microwave, mm-wave high frequency devices (particulary for X-band, k-band and above)

10. Does the Invention possess disadvantages or limitations? Can they be overcome? How?

1.) Technology has yet to be demonstrated. [Laboratory demonstrations proposed and to proceed.]
2.) Throughput limitiations for lateral nanoscale array formation
(Optical feedback and automation approach to be applied.)
3.) Detailed control of nanoscale features required during lateral growth coalescence
(In-situ process control profile approach to be applied.)

11. Enclose sketches, drawings, photographs and other materials that help illustrate the description. (Rough artwork, flow sheets, Polaroid photographs and penciled graphs are satisfactory as long as they tell a clear and understandable story.)
(Attached)

OTHER PERTINENT DATA

1. Is a publication or oral disclosure descriptive of the Invention planned within the next six months? Please give the date (estimate, if known) and attach copies of any existing manuscripts, preprints, abstracts or poster material.

1.) Scientific Publication of Technique and Results Planned
2.) Inclusion in SRC/MARCO Proposal Planned (May 2003)
3.) Inclusion in DARPA Molecular Electronics Proposal Planned
(April 2003)

2. Is there an urgency in making a patent application? If so, please give the likelihood that similar technology may be developed elsewhere. Yes.

1.) LEO Technology Actively Developed at NCSU & Elsewhere (1997-2003)
2.) Edge Defined Lithography Actively Researched and Developed for nanoscale patterning by NCSU, Intel, SCR, SEMATECH, UC Berkeley and Elsewhere
3.) Molecular Electronics actively developed by NCSU, Yale, and elsewhere

4.) Technology has technical need, active research and high visibility (silicon ITRS roadmap, Moore's Law, etc.). This technique, or similar, will likely be developed to fill requirements of Moore's Law.

3. Have any graduate students and/or other technicians been involved in this research? No. At this point the research has only been discussed by faculty members during the preparation of upcoming research proposals.

If so, should the individual(s) be included as a co-inventor? N/A

4. Has the Invention been tested experimentally? Are experimental data or prototypes available?

5. Are there any prior applications for patent by the inventor on this subject? If so, give the serial number(s) and the filing date(s).
Johnson – None
Barlage -
Muth -

6. Are there known inventions by other researchers that are related to this one? Please describe, including information on relevant patents and publications, if available.
LEO and Pendeoepitaxy (GaN) Patents – R. Davis, et. al. (NCSU)
Edge Definition Lithography – C. Osborne (NCSU)

7. Was the work that led to the Invention sponsored by industry or funded by State Federal appropriations? If so, attach a copy of the contract or agreement, if possible, and fill in the appropriate blanks below. One of the below MUST be completed. (This includes the source(s) of funds for the salary of each inventor.)

a. Complete Name of Government Agency:
Contract or Grant No.

b. Name of Industrial Company:

c. Name of Private Sponsor:

d. State or Federal Appropriation: State Salary and Start-Up Funds for Inventors (Idea Conception)

8. Has the Invention been disclosed to industry representatives? Has any commercial interest been shown in it? Please name companies; listing specific individuals and their titles if you know them.
None

a. Do you know of other companies that might be particularly interested in the Invention?
SRC, Sematech, Intel, Motorola, AMD, IBM, Cree, Nitronex, Applied Materials, AMSL, ASM, Lam Research, Micron Technologies, TI, RF Micro Devices, Filtronics, Lucent, JDS Uniphase, TSMC, Sony, Toshiba, NEC, Samsung, Rohm, Matsushita ($>100B market annually in 2008 time horizon)

b. List any manufacturers making comparable equipment or products. Same as Above

c. How much do you estimate your Invention will cost to make? Incremental Cost / Process Change in $1-$10B semiconductor fabrication plant Throughput costs of multiple edge definition steps must be minimized.

Proposed Two-Dimensional Nanoscale Interconnect Arrays for Molecular Electronics Based on Laterally Overgrown III-Nitride Semiconductors

Mark Johnson
Material Science and Engineering
North Carolina State University

March 7, 2003

(DRAFT)

Molecular electronics involves the use of organic molecules as active layer elements for two-terminal and three-terminal devices in digital electronics. As these molecules are inherently 2-5 nm in length, there is the potential for small circuit element features (beyond the limit of silicon CMOS devices). As such, there exists a tremendous driving force for molecular electronic technologies to meet the demands of high-density integrated circuit devices.

In addition to small feature sizes, for molecular electronics to succeed, at least two additional requirements must be met: 1) interconnect technology must be capable of addressing molecular circuit elements on the 2-5nm feature size and 2) parallel fabrication technology must be capable of supporting ~10^{11} molecular elements across a 1 cm^2 chip area. (<100 nm device pitch)

This proposal addresses the development of a wide bandgap semiconductor (GaN and $Al_xGa_{1-x}N$) based interconnect technology for molecular electronics to meet these spatial requirements. Highlights of the proposed techniques are:

1.) Laterally grown GaN interconnect nodes for molecular device attachment.
2.) Nanoscale patterning and feature control on the 2-5nm spatial scale.
3.) Tailored electron affinity and work function enabling molecular contacts through $Al_xGa_{1-x}N$ controlled composition control and doping.
4.) Heterogeneous materials integration with silicon.
5.) Optoelectronic device integration for chip-to-chip communications.

The initial program will address the nanoscale patterning, growth and fabrication of two-terminal and three-terminal interconnect nodes on the 2-5 nm feature size for molecular electronic device element attachment. As shown in Figure 1, the lateral growth of GaN or AlGaN based materials is dominated by the evolution of characteristic facets (habit planes) based on process conditions during epitaxial regrowth.

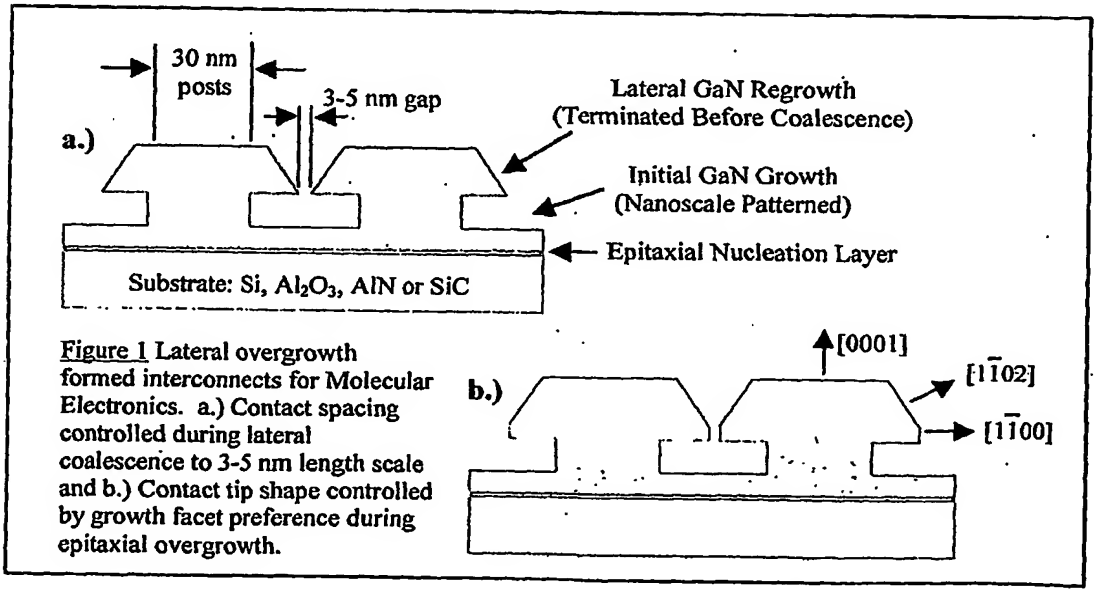

Figure 1 Lateral overgrowth formed interconnects for Molecular Electronics. a.) Contact spacing controlled during lateral coalescence to 3-5 nm length scale and b.) Contact tip shape controlled by growth facet preference during epitaxial overgrowth.

Lateral epitaxial overgrowth (LEO) of GaN was initially developed as a process for the reduction of dislocation defects in epitaxial layers. For dislocation reduction, LEO is done by regrowing GaN across a periodic array of stripes or trenches with a 5-20 micron feature scale. A three to four order of magnitude reduction in dislocation density has been routinely achieved in fully coalesced, laterally overgrown GaN, owing to a combination of the dislocation geometry in the wurtzite crystal structure of GaN and the minimized strain matching required for growth on the [1100] facet of these structures. The LEO process has been a key enabling technology for achieving long lifetime blue laser diodes based on GaN/InGaN heterostructures. (405-410 nm / >10,000 hrs).

While lateral growth has produced significant results in improved crystal quality, lateral growth has not been applied to fabricating three-dimensional active layers or interconnect layers in devices. To address the need of molecular electronics, we propose to extend the lateral growth of GaN in two significant areas. First, we will examine lateral overgrowth on substrates with features on the nanometer spatial scale. As shown in figure 2, we will use edge definition lithography to form a regular array of posts and trenches approximately 30nm wide and 30nm apart. Controlled plasma etching (RIE, ICP, CAIBE) will be used generate a 2:1 aspect ratio of depth to spacing for these trenches. The 30nm spacing is less than the average distance between dislocations in GaN ($\rho = 10^{10}$ /cm^2 $\rightarrow$ d = 0.1 μm). As such, a reduction in dislocation density across the entire GaN layer is also expected. A reduction in trench size and spacing is necessary to reach the high pitch necessary for a molecular electronic interconnects.

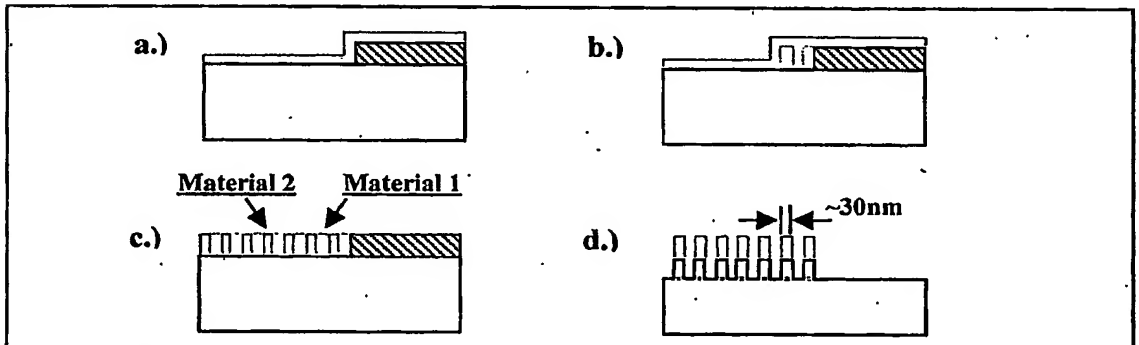

Figure 2 Multiple layered edge definition lithography process sequence for defining a periodic array on the 30nm spatial scale. Two different mask materials, with differential etching capability are deposited in during mask formation. a.) material 1 is deposited isotropically across a field mesa formed by traditional lithography and high angle sidewalls; b.) material 1 is anisotropically removed, leaving only the thicker sidewall mask, with material 2 subsequently deposited across the structure; c.) alternating deposition cycles yields an alternating pattern of material 1 and material 2 (feature width is controlled by alternating layer thicknesses and; d.) Underlying features are formed by preferrential etching of material 2 and subsequent plasma etching of the substrate.

A second requirement is the demonstration of feature control on the 2-5 nm size range. While the spacing between lateral nucleation sites is controlled by the limitations of lithography, the gap or opening between uncoalesced growth fronts is primarily determined by lateral growth rate. Several groups have measured the sidewall surface roughness to be less than 1nm during lateral overgrowth, even though the initial feature

size was several microns across as shown in figure 3. The sub-nanometer degree of spatial variation will be utilized in creating a precise gap for molecular interconnection. Furthermore, the shape of the lateral growth front is determined as a low-index crystal plane, with the surface energy (and resulting habit plane preference) determined primarily by substrate temperature during epitaxial regrowth. A tapered or straight sidewall shape may be formed by judicious control of process parameters as was shown in figure 1. In-situ reflectance difference spectroscopy will be incorporated in epitaxial regrowth to establish an optical signature and thereby control lateral process dimensions during molecular electronic interface fabrication.

Figure 3 AFM image of sidewall surface for laterally overgrown GaN. A surface roughness of less than 1nm is observed. Precise control of sidewall surface morphology is the basis for the nanoscale fabrication dimensions of molecular electronic interconnect arrays.
(R Davis, et. al.)

In addition to linear array fabrication, a two dimensional array of lateral nucleation posts may be used to create a system of interconnect nodes for two-terminal (diode/relay) and three-terminal (gated/transistor) molecular systems. As shown in figure 4, lateral regrowth consists not only on preferred sidewall configuration, but also in planar and azimuthal facet orientation.

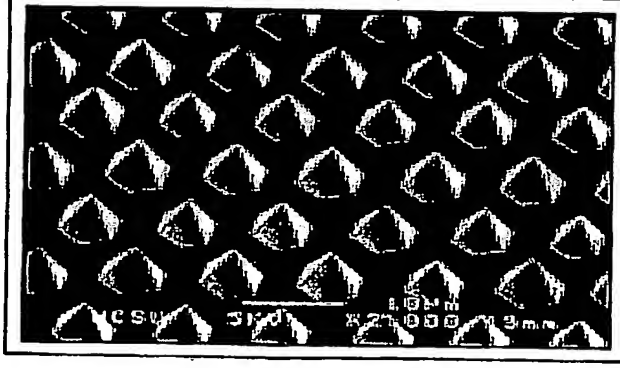

Figure 4 SEM image of laterally overgrown GaN hexagonal pyramid array. This array demonstrates epitaxially controlled facet preference during lateral overgrowth. Dimensions will be controlled for the proposed molecular electronics interconnect array as growth fronts come together and coalesce.
(R Davis, et. al.)

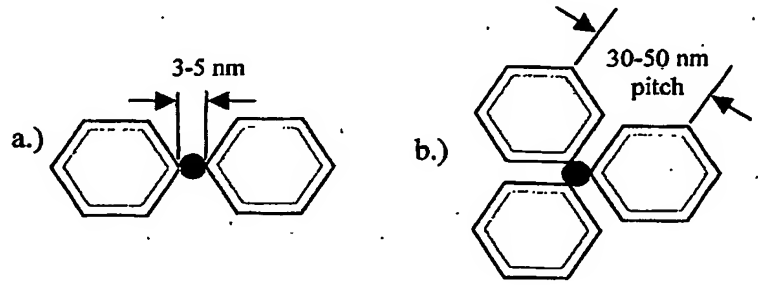

Figure 5 Proposed laterally grown cell geometries for molecular electronic arrays. a.) two- terminal configuration and b.) three terminal configuration. Controlled growth termination during lateral overgrowth matches nanometer scale spaced interconntects. The hexagonal feature size enables a cellular approach to circuit and logic design

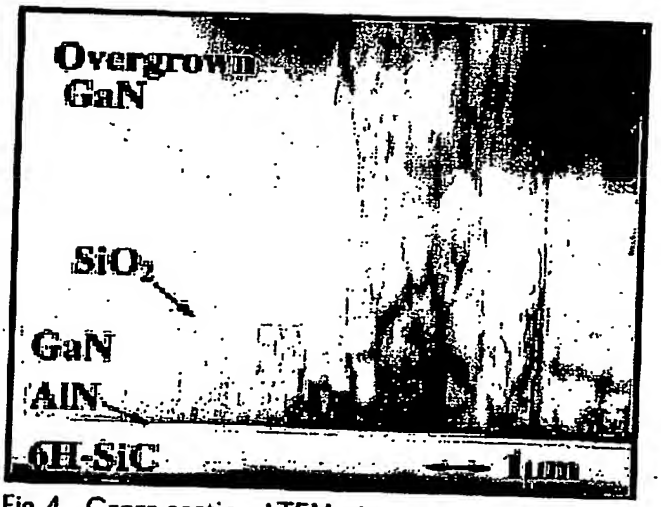

Fig. 4 - Cross-sectional TEM of typical lateral epitaxial overgrowth.

Conduction Band Offset Δ E_c
AlN – GaN = -2.1 eV
AlN – GaAs = -2.8 eV

AlN – Si = -2.8 eV

Bandgap Energy (E_g)
AlN: 6.2 eV
GaN: 3.4 eV
$Al_xGa_{1-x}N$: 6.2(x) + 3.4(1-x) – 1.0 x(1-x)
GaAs: 1.41 eV
Si: 1.1 eV

18 Month Goals

1.) Nanoscale patterning and lateral growth of GaN using edge definition lithography and Metal-Organic Chemical Vapor Deposition (MOCVD).
2.) Nanoscale gap feature formation by lateral overgrowth of GaN
3.) Facet azimuthal controlled growth demonstration for molecular attachment nodes
4.) Lateral Overgrowth of $Al_xGa_{1-x}N$ with nanoscale features for x=0.0 - 0.3.

48 Month Goals

Claims

What is claimed is:

1. A method for forming lateral structures on adjacent decananometer-pitched (5-100nm) devices or mesas comprising:
   (a) fabricating first and second adjacent decananometer-pitched devices or mesas on a substrate, the nanometer-pitched devices being spaced from each other by a predetermined amount to form a trench between the devices on the substrate;
   (b) growing a first lateral structure from the first decananometer-pitched device or mesa in a direction towards the second decananometer-pitched device or mesa; and
   (c) growing a second lateral structure from the second nanometer-pitched device in a direction towards the first nanometer-pitched device, wherein the first and second lateral structures are separated from the substrate by the depth of the trench, the first and second lateral structures substantially cover the trench between the first and second nanometer-pitched devices, and the first and second lateral structures leave a nanometer-pitched (1-50nm) gap between the first and second nanometer-pitched devices or mesas to allow physical interconnection of the devices or mesas via a molecule or heterostructured material.

2. A method for forming a fully coalesced, large-area, low-defect-density substrate materials by laterally growth of a material over a substrate which has been patterned on adjacent decananometer-pitched (5-100nm) trenches, lines or mesas, the method comprising:
   (a) fabricating a plurality of decananometer-pitched mesas or lines on a substrate, the decananometer-pitched mesas or lines being spaced from each other by a predetermined amount to form a trench between the mesas or lines on the substrate;
   (b) fabricating a plurality of decananometer-pitched trenches between lines such that the thickness and the spacing between lines is less than the characteristic dislocation defect density of the substrate;
   (c) epitaxially growing a material on the substrate such that the lateral growth rate exceeds the vertical growth rate; and
   (d) continuing the lateral epitaxial growth on the substrate until lateral growth surfaces coalesce and form a continuous layer over the decananometer-pitched lines, mesas or trenches, whereby the lateral epitaxial growth over the decananometer-pitched lines, mesas or trenches results in a reduction in defect density between the substrate and the continuous layer.

3. A method for fabricating semiconductor devices utilizing decananometer scale (5-100nm) features which have patterning in lines, mesas or trenches and lateral growth of the same or a different semiconductor material as the underlying substrate comprising:
   (a) fabricating individual or a plurality of decananometer-pitched lines or mesas on a substrate, where the substrate comprises a uniform layer or a heterostructure of two or more semiconductor materials;
   (b) laterally growing a first semiconductor material from the decananometer pitched lines;
   (c) laterally growing, from the decananometer pitched lines, a second semiconductor material which has a different characteristic bandgap energy such that quantum confinement occurs in decananometer pitched features of the decananometer pitched lines;
   (d) coalescing a laterally grown semiconductor layer between the decananometer pitched features under conditions such that adjacent lateral growth fronts are non-parallel or parallel; and
   (e) depositing a second semiconductor material on the coalesced layer such that the second semiconductor material fills the non-parallel or parallel space between adjacent decananometer pitched growth surfaces wherein the second semiconductor material has a different bandgap energy from the growth surfaces such that quantum confinement occurs in the material filling the space between adjacent non-paralleo or parallel growth surface fronts.

4. The method of claim 3 further comprising forming semiconductor contacts which are either ohmic or non-ohmic (rectifying) to quantum confined layers formed by the lateral growth of the semiconductor materials from the decananometer features.

5. Electronic, photonic, molecular electronic, spintronic, microfluidic, or micromechanical devices containing layers fabricated using lateral growth of semiconductors from decananometer-spaced features using the process of claim 3.